THE CLAIMS

1-23. (canceled)

24. (Previously presented) A method of forming a floating gate transistor comprising:

forming a source region and a drain region in a substrate;

forming a gate insulator comprising silicon dioxide (SiO2) on a channel region in the substrate between the source region and the drain region; and

forming a floating gate comprising a floating gate material selected from the group consisting of gallium nitride (GaN) and gallium aluminum nitride (GaAlN), such that the floating gate is isolated from conductors and semiconductors.

25. (Previously presented) The method of claim 24 wherein forming a floating gate further comprises forming the floating gate by depositing the floating gate material by metal organic chemical vapor deposition (MOCVD).

26. (Previously presented) The method of claim 24 wherein forming a floating gate further comprises forming the floating gate material by plasma-enhanced molecular beam epitaxy (PEMBE).

27-29. (canceled)

30. (Previously presented) The method of claim 24 wherein:

forming a source region further comprises forming a source region and a drain region in a substrate comprising a substrate material selected from the group consisting of silicon, sapphire, gallium arsenide (GaAs), gallium nitride (GaN), aluminum nitride (AlN), and diamond; and

further comprising:

forming a silicon dioxide (SiO2) intergate insulator on the floating gate; and

forming a control gate on the intergate insulator.

31. (Previously presented) The method of claim 24 wherein forming a floating gate further comprises forming the floating gate by growing gallium nitride (GaN) in a horizontal reactor from trimethyl gallium (TMG), trimethylaluminum (TMA), and ammonia (NH3) source gases and a hydrogen (H2) carrier gas at atmospheric pressure.

32. (Previously presented) A method of forming a floating gate transistor comprising:

forming a gate insulator comprising silicon dioxide (SiO2) on a substrate; and

forming a floating gate on the gate insulator, the floating gate comprising gallium nitride (GaN) or gallium aluminum nitride (GaAlN).

33. (Previously presented) The method of claim 32 wherein:

forming a gate insulator further comprises forming the gate insulator on the substrate comprising a substrate material selected from the group consisting of silicon, sapphire, gallium arsenide (GaAs), gallium nitride (GaN), aluminum nitride (AlN), and diamond; and

further comprising:

forming a source region and a drain region in the substrate;

forming a silicon dioxide (SiO2) intergate insulator on the floating gate; and

forming a control gate on the intergate insulator.

34. (Previously presented) The method of claim 32 wherein forming a floating gate further comprises forming the floating gate by depositing gallium nitride (GaN) on an aluminum nitride (AlN) buffer layer by metal organic chemical vapor deposition (MOCVD).

35. (Previously presented) The method of claim 32 wherein forming a floating gate further comprises forming the floating gate by growing gallium nitride (GaN) in a horizontal reactor from trimethyl gallium (TMG), trimethylaluminum (TMA), and ammonia (NH3) source gases and a hydrogen (H2) carrier gas at atmospheric pressure.

36. (Previously presented) The method of claim 32 wherein forming a floating gate further comprises forming the floating gate by plasma-enhanced molecular beam epitaxy (PEMBE).

37. (Previously presented) A method of forming a floating gate transistor comprising:

forming a source region and a drain region in a substrate;

forming a gate insulator comprising silicon dioxide (SiO2) on a channel region in the substrate between the source region and the drain region; and

forming a floating gate on the gate insulator, the floating gate comprising gallium nitride (GaN) or gallium aluminum nitride (GaAlN).

38. (Previously presented) The method of claim 37 wherein:

forming a source region further comprises forming a source region and a drain region in a substrate comprising a substrate material selected from the group consisting of silicon, sapphire, gallium arsenide (GaAs), gallium nitride (GaN), aluminum nitride (AlN), and diamond; and

further comprising:

forming a silicon dioxide (SiO2) intergate insulator on the floating gate; and

forming a control gate on the intergate insulator.

39. (Previously presented) The method of claim 37 wherein forming a floating gate further comprises forming the floating gate by depositing gallium nitride (GaN) on an aluminum nitride (AlN) buffer layer by metal organic chemical vapor deposition (MOCVD).

40. (Previously presented) The method of claim 37 wherein forming a floating gate further comprises forming the floating gate by growing gallium nitride (GaN) in a horizontal reactor from trimethyl gallium (TMG), trimethylaluminum (TMA), and ammonia (NH3) source gases and a hydrogen (H2) carrier gas at atmospheric pressure.

41. (Previously presented) The method of claim 37 wherein forming a floating gate further comprises forming the floating gate by plasma-enhanced molecular beam epitaxy (PEMBE).

42. (Previously presented) A method of forming a floating gate transistor comprising:

forming a source region and a drain region in a substrate;

forming a gate insulator comprising silicon dioxide (SiO2) on a channel region in the substrate between the source region and the drain region;

forming a floating gate on the gate insulator, the floating gate comprising gallium nitride (GaN) or gallium aluminum nitride (GaAlN);

forming an intergate insulator on the floating gate; and

forming a control gate on the intergate insulator.

43. (Previously presented) The method of claim 42 wherein:

forming a source region further comprises forming a source region and a drain region in a substrate comprising a substrate material selected from the group consisting of silicon, sapphire, gallium arsenide (GaAs), gallium nitride (GaN), aluminum nitride (AlN), and diamond; and

forming an intergate insulator comprises forming a silicon dioxide (SiO2) intergate insulator on the floating gate.

44. (Previously presented) The method of claim 42 wherein forming a floating gate further comprises forming the floating gate by depositing gallium nitride (GaN) on an aluminum nitride (AlN) buffer layer by metal organic chemical vapor deposition (MOCVD).

45. (Previously presented) The method of claim 42 wherein forming a floating gate further comprises forming the floating gate by growing gallium nitride (GaN) in a horizontal reactor from trimethyl gallium (TMG), trimethylaluminum (TMA), and ammonia (NH3) source gases and a hydrogen (H2) carrier gas at atmospheric pressure.

46. (Previously presented) The method of claim 42 wherein forming a floating gate further comprises forming the floating gate by plasma-enhanced molecular beam epitaxy (PEMBE).

47. (Previously presented) A method of forming a floating gate transistor comprising:

forming a gate insulator on a substrate; and

forming a floating gate on the gate insulator, the floating gate comprising gallium aluminum nitride (GaAlN).

48. (Previously presented) The method of claim 47 wherein:

forming a gate insulator further comprises forming the gate insulator comprising silicon dioxide (SiO2) on the substrate comprising a substrate material selected from the group consisting of silicon, sapphire, gallium arsenide (GaAs), gallium nitride (GaN), aluminum nitride (AlN), and diamond; and

further comprising:

forming a source region and a drain region in the substrate;

forming a silicon dioxide (SiO2) intergate insulator on the floating gate; and

forming a control gate on the intergate insulator.

49. (Previously presented) The method of claim 47 wherein forming a floating gate further comprises forming the floating gate by depositing gallium nitride (GaN) on an aluminum nitride (AlN) buffer layer by metal organic chemical vapor deposition (MOCVD).

50. (Previously presented) The method of claim 47 wherein forming a floating gate further comprises forming the floating gate by growing gallium nitride (GaN) in a horizontal reactor from trimethyl gallium (TMG), trimethylaluminum (TMA), and ammonia (NH3) source gases and a hydrogen (H2) carrier gas at atmospheric pressure.

51. (Previously presented) The method of claim 47 wherein forming a floating gate further comprises forming the floating gate by plasma-enhanced molecular beam epitaxy (PEMBE).

52. (Previously presented) A method of forming a floating gate transistor comprising:

forming a source region and a drain region in a substrate;

forming a gate insulator on a channel region in the substrate between the source region and the drain region; and

forming a floating gate on the gate insulator, the floating gate comprising gallium aluminum nitride (GaAlN).

53. (Previously presented) The method of claim 52 wherein:

forming a source region further comprises forming a source region and a drain region in a substrate comprising a substrate material selected from the group consisting of silicon, sapphire, gallium arsenide (GaAs), gallium nitride (GaN), aluminum nitride (AlN), and diamond;

forming a gate insulator further comprises forming the gate insulator comprising silicon dioxide (SiO2); and

further comprising:

forming a silicon dioxide (SiO2) intergate insulator on the floating gate; and

forming a control gate on the intergate insulator.

54. (Previously presented) The method of claim 52 wherein forming a floating gate further comprises forming the floating gate by depositing gallium nitride (GaN) on an aluminum nitride (AlN) buffer layer by metal organic chemical vapor deposition (MOCVD).

55. (Previously presented) The method of claim 52 wherein forming a floating gate further comprises forming the floating gate by growing gallium nitride (GaN) in a horizontal reactor from trimethyl gallium (TMG), trimethylaluminum (TMA), and ammonia (NH3) source gases and a hydrogen (H2) carrier gas at atmospheric pressure.

56. (Previously presented) The method of claim 52 wherein forming a floating gate further comprises forming the floating gate by plasma-enhanced molecular beam epitaxy (PEMBE).

57. (Previously presented) A method of forming a floating gate transistor comprising:

forming a source region and a drain region in a substrate;

forming a gate insulator on a channel region in the substrate between the source region and the drain region;

forming a floating gate on the gate insulator, the floating gate comprising gallium aluminum nitride (GaAlN);

forming an intergate insulator on the floating gate; and

forming a control gate on the intergate insulator.

58. (Previously presented) The method of claim 57 wherein:

forming a source region further comprises forming a source region and a drain region in a substrate comprising a substrate material selected from the group consisting of silicon, sapphire, gallium arsenide (GaAs), gallium nitride (GaN), aluminum nitride (AlN), and diamond; and

forming a gate insulator further comprises forming the gate insulator comprising silicon dioxide (SiO2); and

forming an intergate insulator comprises forming a silicon dioxide (SiO2) intergate insulator on the floating gate.

59. (Previously presented) The method of claim 57 wherein forming a floating gate further comprises forming the floating gate by depositing gallium nitride (GaN) on an aluminum nitride (AlN) buffer layer by metal organic chemical vapor deposition (MOCVD).

60. (Previously presented) The method of claim 57 wherein forming a floating gate further comprises forming the floating gate by growing gallium nitride (GaN) in a horizontal reactor from trimethyl gallium (TMG), trimethylaluminum (TMA), and ammonia (NH3) source gases and a hydrogen (H2) carrier gas at atmospheric pressure.

61. (Previously presented) The method of claim 57 wherein forming a floating gate further comprises forming the floating gate by plasma-enhanced molecular beam epitaxy (PEMBE).